

Anschlußbelegung des Pollin-Funk-Eval. Boards:

Funkmodule	Tiny3213	Mega8	Mega16/32
nINT/VDI	PB0 (AIN0)	PB0 (ICP)	PB0 (T0)
SDI	PB5 (MOSI)	PB3 (MOSI/OC)	PB5 (MOSI)
SCK	PB7 (SCK)	PB5 (SCK)	PB7 (SCK)
nSEL	PB4	PB2 (SS/OC1B)	PB4 (SS)
SDO	PB6 (MISO)	PB4 (MISO)	PB6 (MISO)
nIRQ	PD2 (INT0)	PD2 (INT0)	PD2 (INT0)
FSK/DATA/nFFS	PB3 (OCI)	PD7 (AINT)	PB3 (AINT)
DCLK/CFIL/FFIT	PD3 (INT1)	PD3 (INT1)	PD3 (INT1)
CLK	-	{neu: PD5 (T1)}	{neu: PB1 (T1)}
nRES	-	-	-
GND	GND	GND	GND
VDD	VCC	VCC	VCC

Definition	Funktion	Type
nINT/VDI	Interrupt input (active low) / Valid data indicator	DI/DO
SDI	SPI data input	DI
SCK	SPI clock input	DI
nSEL	Chip select (active low)	DI
SDO	Serial data output with bus hold	DO
nIRQ	Interrupts request output (active low)	DO
FSK/DATA/nFFS	Transmit FSK data input / received data output (FIFO not used) / FIFO select	DI/DO/DI
DCLK/CFIL/FFIT	Clock output (no FIFO) /external filter capacitor (analog mode) / FIFO interrupts (active high) when FIFO level set to 1, FIFO empty interruption can be achieved	DO/AIO/DO
CLK	Clock output for external microcontroller	DO
nRES	Reset output (active low)	
GND	Power ground	S
VDD	Positive power supply	S

Control Interface:

Kommandos werden seriell über die SPI Schnittstelle übertragen. Die Bits werden an den Baustein bei steigender Flanke des Taktsignals am SCK Pin übertragen. Wenn das nSEL Signal (select slave) high wird, wird das serielle Interface initialisiert. Das bedeutet, dass man vor jedem Kommando an den Baustein den nSel Pin auf Low legen muß und nach der Übermittlung wieder auf High.

POR	Power on reset
IT	Interrupt request

Beschreibung der Kontroll Kommandos:

1. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	0	0	el	ef	b1	b0	x3	x2	x1	x0	8008H

- Bit el aktiviert das interne Datenregister. Wenn dieses Register aktiv ist, muß der FSK-Pin auf Logic High Level gelegt werden.
- Bit ef aktiviert den FIFO Modus. Wenn ef=0 dann werden Pin 6 (DATA) und Pin7 (DCLK) für die Datenausgabe verwendet

b1	b0	F ¹ [MHz]
0	0	315
0	1	433
1	0	868
1	1	915

x3	x2	x1	x0	CLC ² [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10
0	1	0	0	10.5
0	1	0	1	11.0
0	1	1	0	11.5
0	1	1	1	12.0
1	0	0	0	12.5
1	0	0	1	13.0
1	0	1	0	13.5
1	0	1	1	14.0
1	1	0	0	14.5
1	1	0	1	15.0
1	1	1	0	15.5
1	1	1	1	16.0

¹ Frequency Band

² Crystal Load Capacitance

PDIP

(XCK/T0) PB0	1	40	PA0 (ADC0)
(T1) PB1	2	39	PA1 (ADC1)
(INT2/AIN0) PB2	3	38	PA2 (ADC2)
(OC0/AIN1) PB3	4	37	PA3 (ADC3)
(SS) PB4	5	36	PA4 (ADC4)
(MOSI) PB5	6	35	PA5 (ADC5)
(MISO) PB6	7	34	PA6 (ADC6)
(SCK) PB7	8	33	PA7 (ADC7)
RESET	9	32	AREF
VCC	10	31	GND
GND	11	30	AVCC
XTAL2	12	29	PC7 (TOSC2)
XTAL1	13	28	PC6 (TOSC1)
(RXD) PD0	14	27	PC5 (TDI)
(TXD) PD1	15	26	PC4 (TDO)
(INT0) PD2	16	25	PC3 (TMS)
(INT1) PD3	17	24	PC2 (TCK)
(OC1B) PD4	18	23	PC1 (SDA)
(OC1A) PD5	19	22	PC0 (SCL)
(ICP1) PD6	20	21	PD7 (OC2)

PDIP

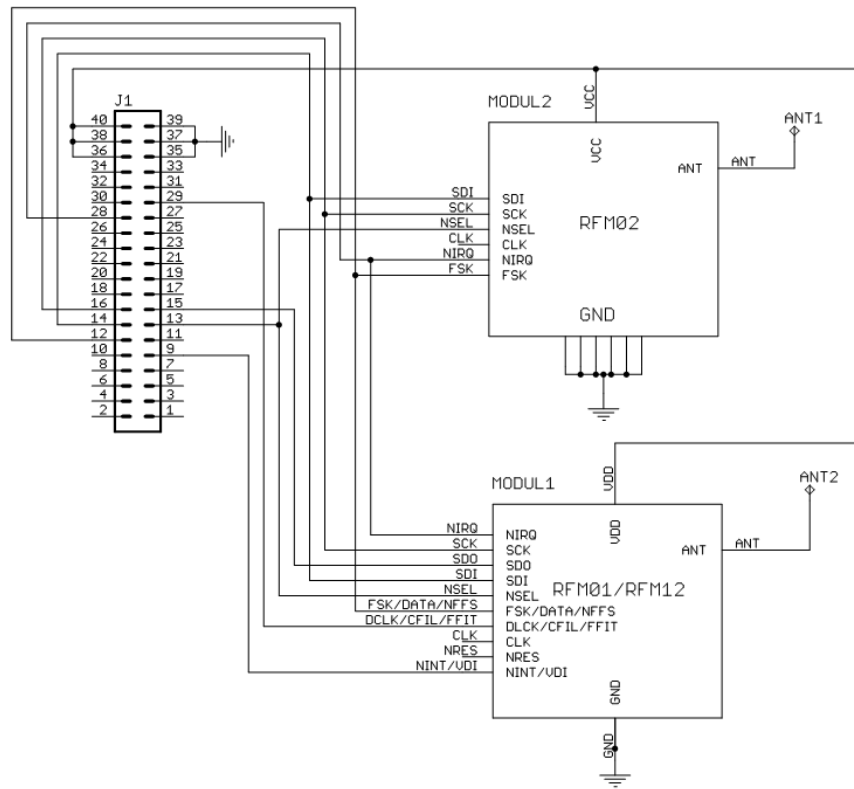
(RESET) PC6	1	28	PC5 (ADC5/SCL)
(RXD) PD0	2	27	PC4 (ADC4/SDA)
(TXD) PD1	3	26	PC3 (ADC3)
(INT0) PD2	4	25	PC2 (ADC2)
(INT1) PD3	5	24	PC1 (ADC1)
(XCK/T0) PD4	6	23	PC0 (ADC0)
VCC	7	22	GND
GND	8	21	AREF
(XTAL1/TOSC1) PB6	9	20	AVCC
(XTAL2/TOSC2) PB7	10	19	PB5 (SCK)
(T1) PD5	11	18	PB4 (MISO)
(AIN0) PD6	12	17	PB3 (MOSI/OC2)
(AIN1) PD7	13	16	PB2 (SS/OC1B)
(ICP1) PB0	14	15	PB1 (OC1A)

Jumperbelegung des Pollin ATMEGA Evaluationsboards:

Jumper-Funktionen JP1 - JP12

Jumper	Funktion	Pin an ATmega16/32/8535	Pin an ATmega8	Pin an ATtiny2313
JP1	UART RX	14 - PD0 (RX)	2 - PD0 (RX)	2 - PD0 (RX)
JP2	UART TX	15 - PD1 (TX)	3 - PD1 (TX)	3 - PD1 (TX)
JP3	Taster 1	16 - PD2 (INT0)	4 - PD2 (INT0)	6 - PD2 (INT0)
JP4	Taster 2	17 - PD3 (INT1)	5 - PD3 (INT1)	7 - PD3 (INT1)
JP5	Taster 3	18 - PD4 (OC1B)	6 - PD4 (XCK/T0)	8 - PD4 (INT1)
JP6	LED 1	19 - PD5 (OC1A)	11 - PD5 (T1)	9 - PD5 (T1)
JP7	LED 2	20 - PD6 (ICP)	12 - PD6 (AIN0)	11 - PD6 (ICP)
JP8	AC-Summer	21 - PD7 (OC2)	13 - PD7 (AIN1)	n.c.
JP9	I2C-Data	23 - PC1	n.c.	n.c.
JP10	I2C-Clock	22 - PC0	n.c.	n.c.
JP11	I2C-Data	kein I2C	27 - PC4 (ADC4/SDA)	n.c.
JP12	I2C-Clock	kein I2C	28 - PC5 (ADC5/SCL)	n.c.

Schaltplan für den Funkmodul-Adapter-433:



Belegung Pfostenleiste J1:

(Restliche Pins auf Wannensteckerleiste J1 sind nicht angeschlossen)

J1	Funkmodule	Tiny 2313	Mega 8	Mega16/32
9	NINT	PB0	PB0	PB0
12	FSK	PB3	PD7	PB3
13	NSEL	PB4	PB2	PB4
14	SDI	PB5	PB3	PB5
15	SDO	PB6	PB4	PB6
16	SCK	PB7	PB5	PB7
28	NIRQ	PD2	PD2	PD2
29	DCLK	PD3	PD3	PD3
36,38,40	VCC	VCC	VCC	VCC

Definition	Funktion	Type
nINT	Interrupt input (active low)	DI
VDI	Valid data indicator	DO
SDI	SPI data input	DI
SCK	SPI clock input	DI
nSEL	Chip select (active low)	DI
SDO	Serial data output with bus hold	DO
nIRQ	Interrupts request output (active low)	DO
FSK	Transmit FSK data input	DI
DATA	Received data output (FIFO not used)	DO
nFFS	FIFO select	DI
DCLK	Clock output (no FIFO)	DO
CFIL	external filter capacitor (analog mode)	AIO
FFIT	FIFO interrupts (active high) when FIFO level set to 1, FIFO empty interruption can be achieved	DO
CLK	Clock output for external microcontroller	DO
nRES	Reset output (active low)	
GND	Power ground	S
VDD	Positive power supply	S

Mega8:

J1	RFM12		Mega8			
Pin	Funct.	Dir	Pin	Funct.	Dir	Description
9	nInt	DI	PB0	ICP1	DO	
13	nSel	DI	PB2	SS/OC1B	DO	SelectSlave
14	SDI	DI	PB3	MOSI/OC1	DO	
15	SDO	DO	PB4	MISO	DI	
16	SCK	DI	PB5	SCK	DO	
28	nIRQ	DO	PD2	INT0	DI	
29	DCLK	DO	PD3	INT1	DI	
12	FSK	DI	PD7	AIN1	DO	
36,38,40	VCC		VCC	VCC		

Mega16:

J1	RFM12		Mega16			
Pin	Funct.	Dir	Pin	Funct.	Dir	Description
9	nInt	DI	PB0	ICP1	DO	
12	FSK	DI	PB3	AIN1	DO	
13	nSel	DI	PB4	SS/OC1B	DO	SelectSlave
14	SDI	DI	PB5	MOSI/OC1	DO	
15	SDO	DO	PB6	MISO	DI	
16	SCK	DI	PB7	SCK	DO	
28	nIRQ	DO	PD2	INT0	DI	
29	DCLK	DO	PD3	INT1	DI	
36,38,40	VCC		VCC	VCC		